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Study of the Complexity of CMOS Neural Network Implementations Featuring Heart Rate Detection

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Plan

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Plan

1. Introduction
2. Artificial Intelligence on the Edge
3. Artificial Neural Network
4. CMOS preprocessor
5. Summary and results

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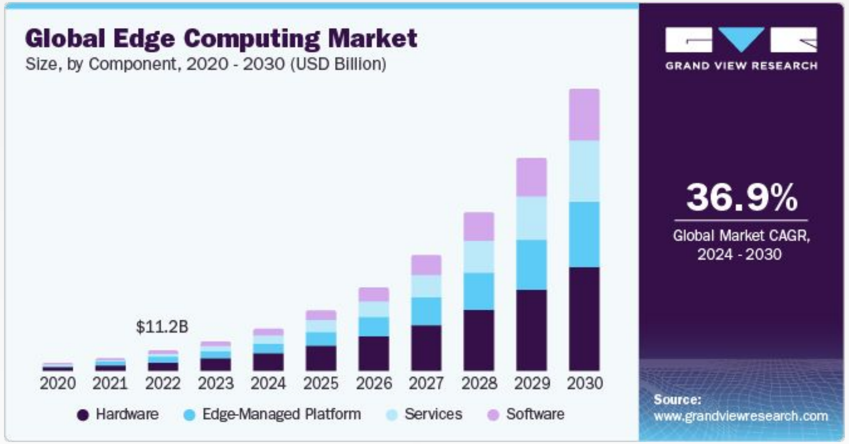
Motivation

- Increasing popularity of edge computing
- Rise of IoT
- Network congestion and bandwidth limitations



Objectives

1. Implement and train an ANN
2. Design a CMOS preprocessor that will behave identically to the ANN
3. Optimize both the ANN and the preprocessor to reduce overall complexity

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Challenges

- Performance-complexity trade-off
- Weight constraints
- Custom activation function as a requirement
- ANN -> CMOS conversion

Edge AI

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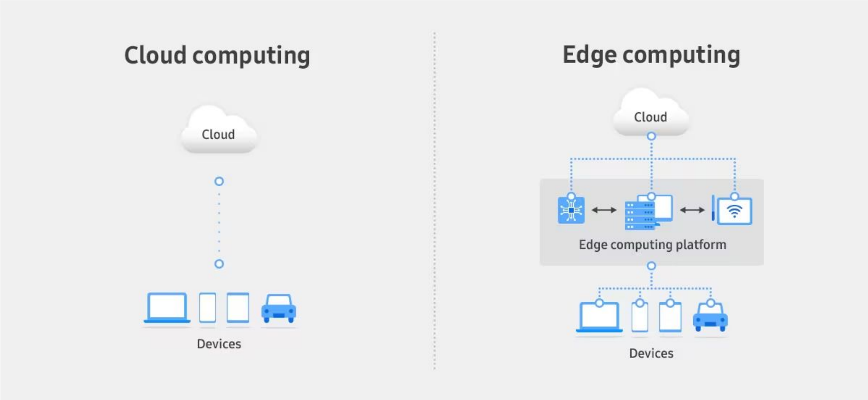
Edge vs Cloud Computing

- Both approaches leverage delegating processing to external nodes / devices
  - … though there are substantial differences
- Both approaches are commonly used in the Big Data world



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Why bother?

- Rapid development in AI accelerating technologies
- Privacy and security concerns
- Offline capabilities
- Not all ML problems require complex models

"The simpler it is, the better I like it."
~ Peter Lynch

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Artificial Neural Network

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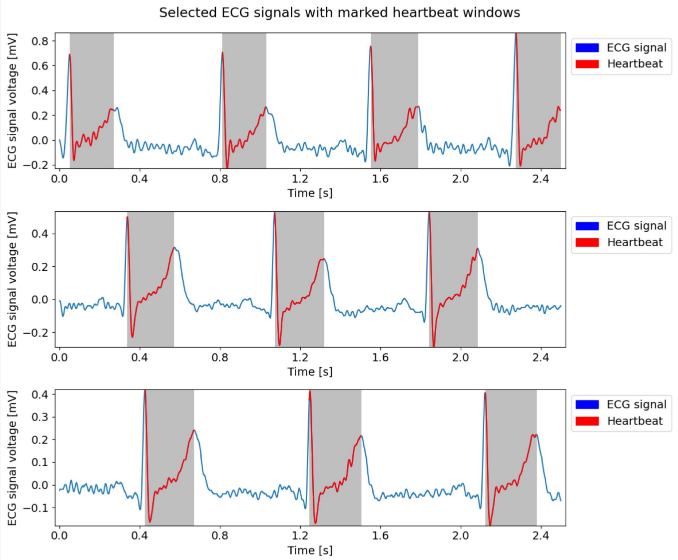
ANN - Dataset

- ECG-ID database, available on PhysioNet (manual adjustments were necessary)
- ECG signals with windows classified as heartbeat or non-heartbeat
- Window size and sampling frequency as hyperparameters



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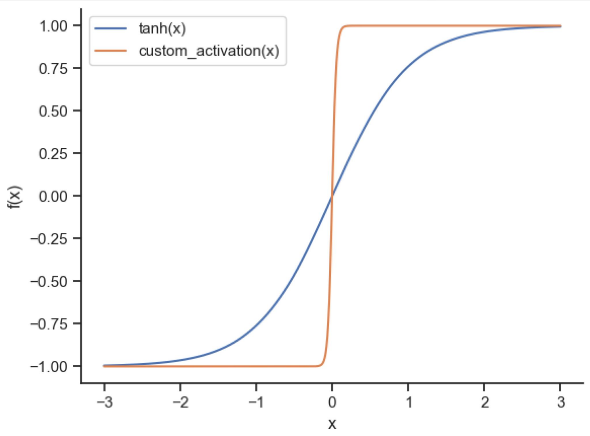
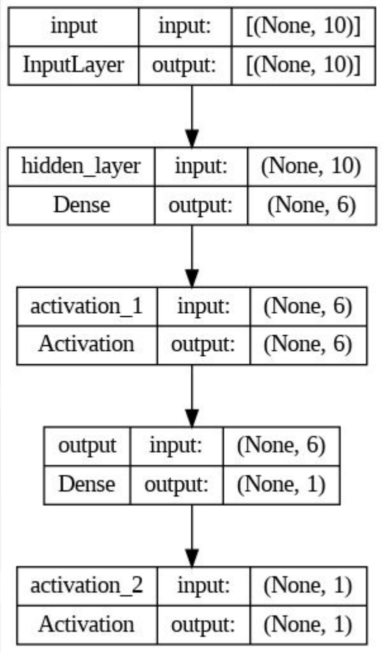
ANN - Architecture

- One hidden layer
- Custom sigmoidal activation function





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CMOS Preprocessor

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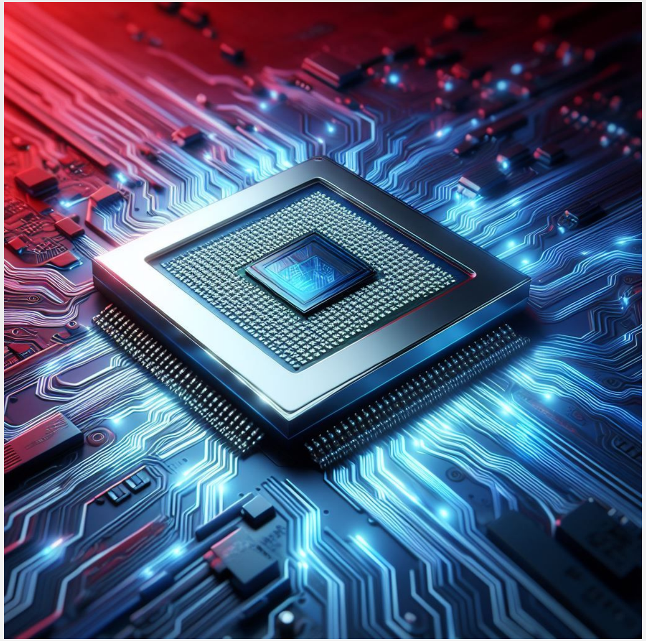
Hardware Complexity

Technology:

- TSMC Taiwan Semiconductor 65 nm CMOS technology
- Weak inversion mode

Hardware metrics:

- Number of transistors
- Active Area [mm^2]
- Maximum processing speed [samples / s]
- Maximum power consumption [nW]



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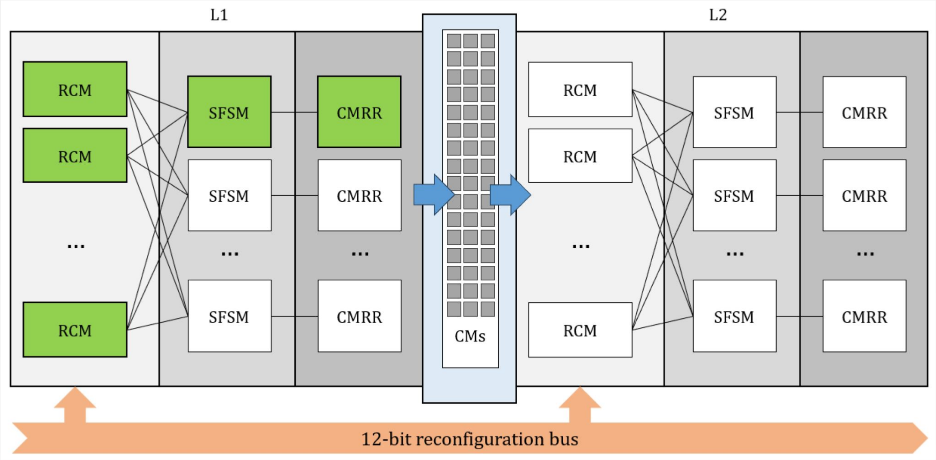
Preprocessor - architecture



- Current Mirror (CM)
- Reconfigurable Current Mirror (RCM)
- Sigmoidal Function Shaping Module (SFSM)
- Common Mode Rejection Ratio (CMRR)

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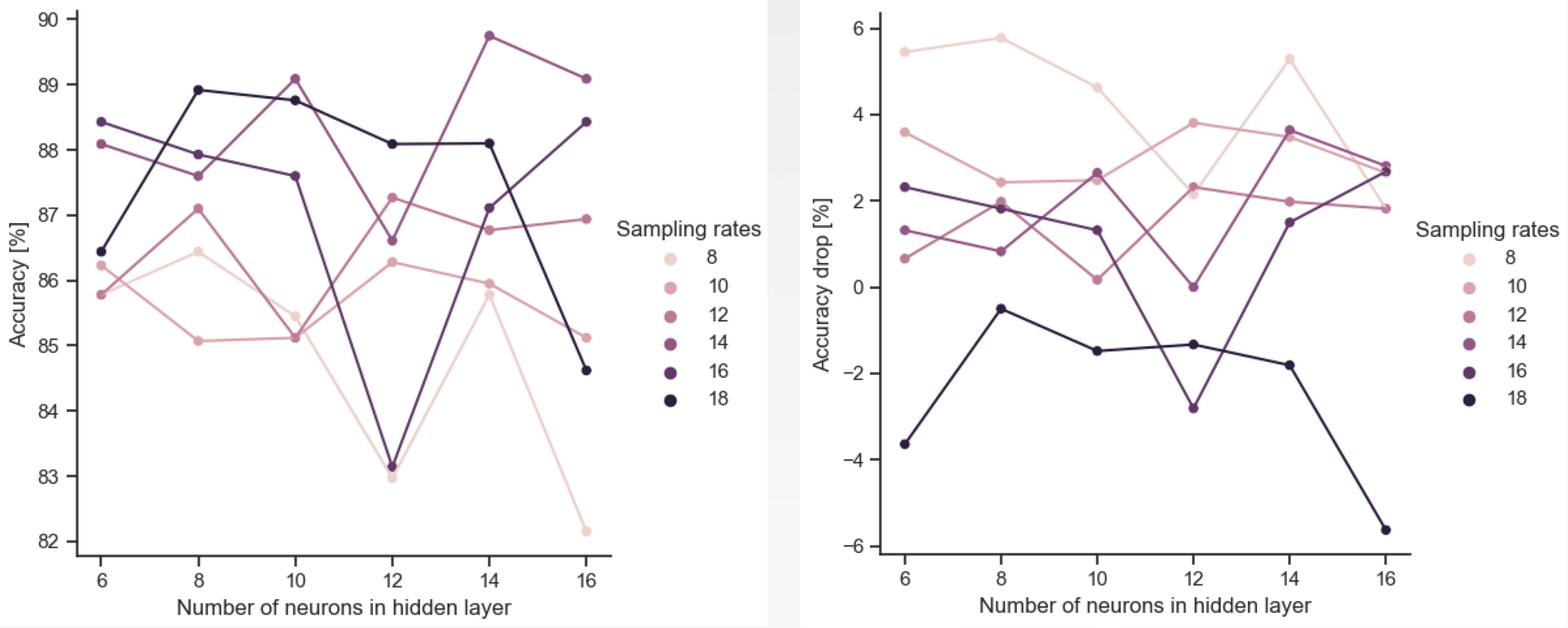

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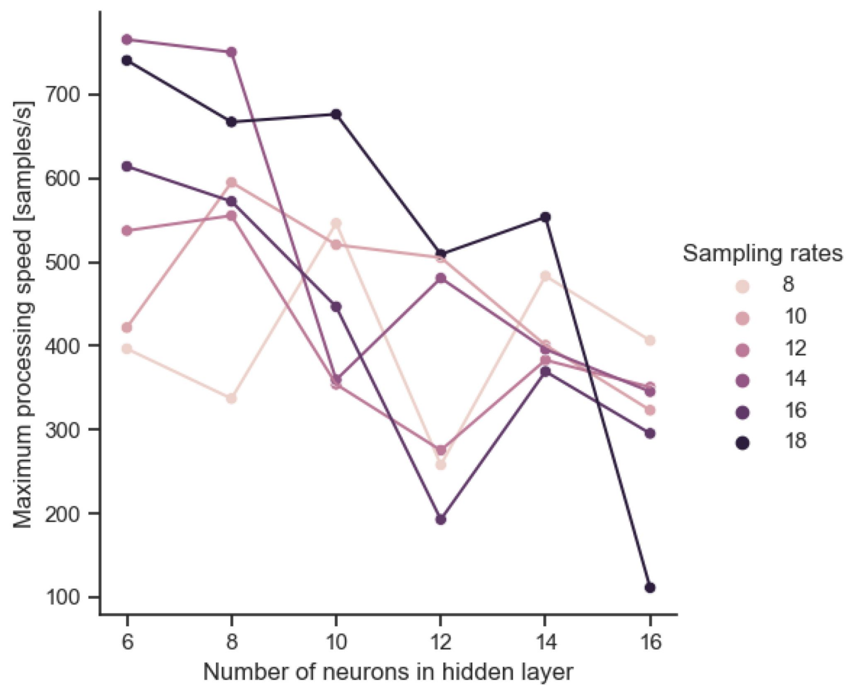

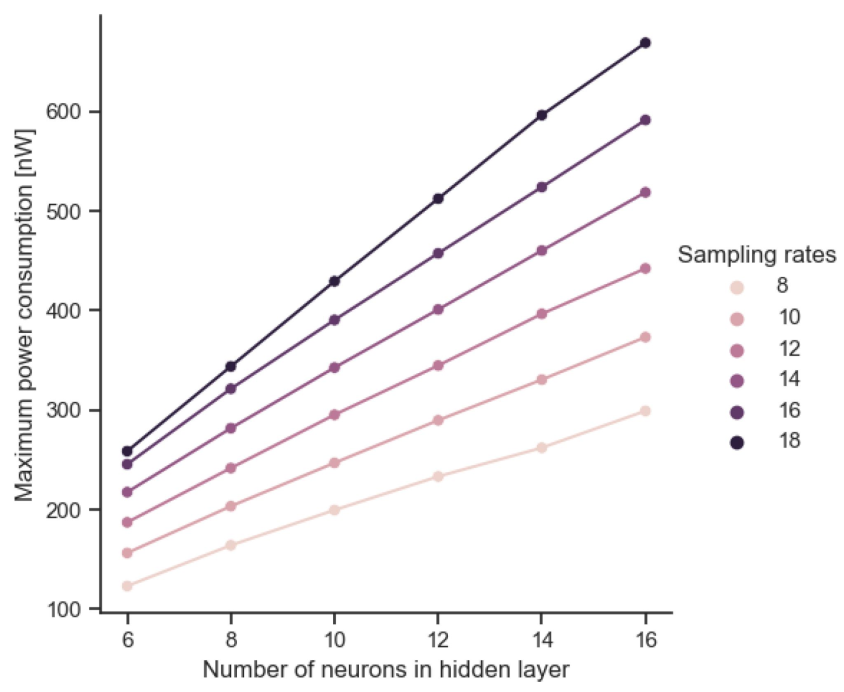

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Conclusions

- We successfully implemented a Deep Learning model with high accuracy and minimal number of parameters.
- It is feasible to develop CMOS preprocessor based on Neural Networks without experiencing a significant loss of accuracy.
- The ASIC design can utilize human energy-harvesting cells for power generation.

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Thank you for your attention